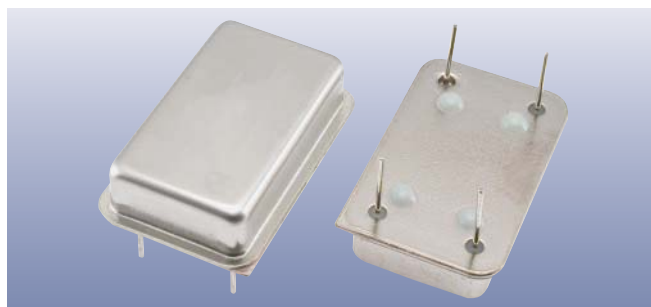


PIN	CONNECTION
1	Enable / disable or Freq adjustment
7	Ground
8	Output
14	Supply

Features

- ▶ 3.3V Stratum 3 compliant (VC)TCXO
- ▶ CMOS output
- ▶ Suitable as SONET/SDH timing source
- ▶ Excellent frequency stability
- ▶ Low jitter

Enable / Disable Function (HTFL)

Input (pin 1)	Output (pin 8)
Open	Enabled
'1' level	Enabled
'0' level	High Impedance

Specifications

Parameters	Product		Option Codes
	HTFL	HTVL	
Frequency range: 6.40 ~ 56.0MHz	■	■	
Calibration tolerance: ±1.0ppm	■	■	
Frequency stability: ±4.6ppm (inclusive of calibration tolerance temperature, voltage, load, 20years ageing, shock & vibration)	■	■	
Temperature range: 0 to +70°C -40 to +85°C	■ □	■ □	5 6
Storage temperature range: -55 to +125°C	■	■	
Temperature stability: ±0.5ppm ±1.0ppm other	□ ■ □	□ ■ □	E F specify
Supply voltage (V _{DD}): +3.3V (±5%)	■	■	
Supply current (6.4~52.0MHz): 10mA max	■	■	
Driving ability: 15pF CMOS	■	■	
Logic levels: '0' level = 10%V _{DD} max '1' level = 90%V _{DD} min	■ ■	■ ■	
Output current: '0' level = 4.0mA '1' level = -4.0mA	■ ■	■ ■	
Waveform symmetry: 45:55 max at 50%V _{DD}	■	■	
Rise / fall time: 8ns max	■	■	
Frequency adjustment: None ±10ppm min, +1.65V ±1.35V >100kΩ input impedance ±5% linearity	■	■ ■ ■	
Enable / disable function: None Tristate (control via pin 1) (V _{IH} =70%V _{DD} min, V _{IL} =30%V _{DD} max)	■	■	
Phase noise: -50dBc/Hz typ @ 1Hz -80dBc/Hz typ @ 10Hz -110dBc/Hz typ @ 100Hz -135dBc/Hz typ @ 1kHz -150dBc/Hz typ @ 10kHz -150dBc/Hz typ @ 100kHz	■ ■ ■ ■ ■ ■	■ ■ ■ ■ ■ ■	
Period jitter RMS: 3ps max	■	■	
Phase jitter RMS: 1.0ps max, 12kHz~f _o /2 3.0ps max, 10Hz~f _o /2	■ ■	■ ■	
TDEV: 1.0ns max over 1 sec 2.0ns max over 4 sec	■ ■	■ ■	

■ Standard. □ Optional - Please specify required code(s) when ordering

Ordering Information

Product name + option codes + frequency

eg: HTFL/5F 19.440MHz ±1.0ppm, 0+70°C, TCXO no VC

HTVL/6E 44.7360MHz ±0.5ppm, -40+85°C, TCXO with VC

Option code X (eg HTVL/X) denotes a custom spec.